ABSTRACT OF THE DISCLOSURE

A method is provided for forming a stacked-gate flash memory cell having a shallow trench isolation with a high-step of oxide and high lateral coupling. This is accomplished by first depositing an unconventionally high or thick layer of nitride and then forming a shallow trench isolation (STI) through the nitride layer into the substrate , filling the STI with isolation oxide, removing the nitride thus leaving behind a deep opening about the filled STI, filling conformally the opening with a first polysilicon layer to form a floating gate, forming interpoly oxide layer over the floating gate, and then forming a second polysilicon layer to form the control gate and finally forming the self-aligned source of the stacked-gate flash memory cell of the invention. A stacked-gate flash memory cell is also provided having a shallow trench isolation with a high-step of oxide and high lateral coupling.